

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Previously Presented) A digital processing system having
2 a microprocessor, wherein the microprocessor comprises:

3 fetch circuitry for fetching instruction fetch packets from
4 sequential memory address locations, wherein each fetch packet
5 contains a first plurality of fixed and equal length instructions,
6 each instruction including an instruction type and a predetermined
7 p-bit, said p-bit having a first digital state indicating a next
8 instruction is to execute in parallel with said instruction and a
9 second digital state indicating a next instruction is to execute in
10 a cycle after said instruction;

11 a second plurality of functional units, each of the second
12 plurality of functional units operable to execute a corresponding
13 instruction in parallel with other functional units, and

14 dispatch circuitry connected to said fetch circuitry and said
15 second plurality of functional units operable to

16 select an execute packet from two fetch packets, wherein
17 an execute packet varies in size and contains only a set of
18 instructions that can be executed in parallel on the plurality
19 of functional units, by scanning instructions from lower
20 memory address locations to higher memory address locations
21 beginning in a first fetch packet, adding an instruction to
22 said execute packet when said p-bit of a prior instruction has
23 said first digital state and continuing past an end of said
24 first fetch packet to a beginning of a second fetch packet
25 until said p-bit of an instruction has said second digital
26 state, and

27 dispatch each instruction of said selected execute packet
28 to a functional unit corresponding to said instruction type of
29 said instruction,

30 wherein the dispatch circuitry comprises:

31 a first latch to hold said first plurality of
32 instructions of a first fetch packet, said first latch
33 including a first plurality of sections, each section storing
34 a corresponding one of said first plurality of instructions of
35 said first fetch packet;

36 a second latch to hold said first plurality of
37 instructions of a second fetch packet immediately following
38 said first fetch packet, said second latch including a first
39 plurality of sections, each section storing a corresponding
40 one of said first plurality of instructions of said second
41 fetch packet;

42 a first plurality of multiplexers, each multiplexer
43 having exactly two data inputs, a first data input receiving
44 an entire instruction from a predetermined section of said
45 first latch and a second data input receiving an entire
46 instruction from a corresponding section of said second latch,
47 a control input and an output, each multiplexer selecting at
48 said output either said entire instruction from said section
49 of said first latch, said entire instruction from said section
50 of said second latch, or no instruction, dependent upon said
51 control input;

52 a dispatch control circuit connected to said first latch,
53 said second latch, and said plurality of multiplexers, said
54 dispatch control circuit receiving said predetermined p-bit
55 from each instruction of said first latch and each instruction
56 of said second latch for control of said plurality of
57 multiplexers via said control inputs according to the execute
58 packets determined by only said p-bits; and

59 a cross point circuitry connected to said outputs of said
60 plurality of multiplexers for dispatching said instructions at
61 said output of said multiplexers to a functional unit
62 corresponding to said instruction type of each instruction.

Claims 2 to 6 (Canceled)

1 7. (Currently Amended) A method of operating a digital
2 system having a microprocessor, wherein the microprocessor has a
3 plurality of functional units for executing instructions in
4 parallel, comprising the steps of:
5 storing fixed and equal length instructions at sequential
6 memory address locations, each instruction including an instruction
7 type and a predetermined p-bit, said p-bit having a first digital
8 state indicating a next instruction is to execute in parallel with
9 said instruction and a second digital state indicating a next
10 instruction is to execute in a cycle after said instruction;
11 fetching a sequence of instruction fetch packets, wherein each
12 fetch packet contains a first plurality of instructions;
13 scanning the p-bit of each instruction of each fetch packet
14 from lowest memory address location in a first memory fetch packet
15 to highest memory address location in a second immediately
16 following fetch packet to determine an execute packet dependent on
17 the p-bits, wherein said step of determining an execute packet
18 boundary dependent upon the p-bits includes
19 storing each instruction of said first fetch packet in a
20 corresponding section of a first latch,
21 storing each instruction of said second fetch packet in a
22 corresponding section a second latch, and
23 selecting only ~~either~~ one output from among the set
24 consisting of an entire instruction from a predetermined
25 section of said first latch, an entire instruction from a

26 corresponding section of said second latch, ~~or~~ and no
27 instruction, dependent upon only said p-bit from each
28 instruction stored in said first latch and each instruction
29 stored in said second latch; and
30 dispatching each selected instruction within the determined
31 execute packet to one of a second plurality of execution units
32 dependent upon an instruction type of the instruction.

Claims 8 to 11. (Canceled)